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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,204	09/22/2003	Gang Wang	031188	5746

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EXAMINER	
SEFER, AHMED N	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 11/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/665,204	WANG ET AL.	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/19/2005 has been entered.

Allowable Subject Matter

2. The indicated allowability of claims 1-16 is withdrawn in view of the newly discovered reference(s) to Nishikata ("Nishikata") USPN 5,998,851 and Uchida et al. ("Uchida") US PG-Pub 2001/0048118. Rejections based on the newly cited reference(s) follow.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, **a semiconductor optical waveguide path** (claim 10) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must

be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The disclosure is objected to because of the following informalities: In the last line of claim 8, the recitation calling for "the buffer layer In.sub.1xGa.sub.xAs.sub.yP.sub.1-Y (0 x 1, 0 y 1)" is not disclosed. The specification merely discloses an InP buffer.

Claim Objections

5. Claim 8 is objected to because of the following informalities: The recitation calling for "the buffer layer In.sub.1xGa.sub.xAs.sub.yP.sub.1-Y **(0 x 1, 0 y 1)**" should read "the buffer layer In.sub.1xGa.sub.xAs.sub.yP.sub.1-Y **($0 \leq x \leq 1$, $0 \leq y \leq 1$)**". Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claim 16 is rejected under 35 U.S.C. 102(b) as being anticipated by Nishikata.

Nishikata discloses (fig. 5 and col. 5, lines 25-40) a semiconductor light-receiving device comprising: a semiconductor substrate 11 of a first conductivity type; a buffer layer of the first conductivity type 12 that is formed on the semiconductor substrate and has a lower impurity concentration than the semiconductor substrate; a light absorption layer 14 that is formed on the buffer layer and generates carriers in accordance with incident light; a semiconductor layer 16 of a second conductivity type that is formed on the light absorption layer; and a semiconductor intermediate layer 13 that is interposed between the buffer layer and the light absorption layer, and has a forbidden bandwidth within a range lying between the forbidden bandwidth of the buffer layer and the forbidden bandwidth of the light absorption layer.

8. Claims 17-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Buchanan et al. (" Buchanan") US PG-Pub 2003/0211648.

Buchanan discloses in fig. 7 a semiconductor light-receiving device comprising: a semi-insulating substrate 1; a semiconductor layer 5 of a first conduction type that is formed on the semi-insulating substrate; a buffer layer 4g of the first conduction type that is formed on the semiconductor layer; a light absorption layer 4e that is formed on the buffer layer and generates carriers in accordance with incident light; a semiconductor layer of a second conduction type 3 that is formed on the light absorption layer; a high-concentration semiconductor intermediate tunneling layer 4f of the first conduction type that is interposed between the buffer layer and the

light absorption layer having a higher impurity concentration than the buffer layer and a thickness and impurity concentration within the recited range (as in claim 19).

As to the semiconductor intermediate tunneling layer allowing electrons to pass therethrough to the buffer layer due to tunnel effect, it is a desired result rather than a structural limitation. See In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997); See also In re Swinehart, 439 F.2d210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971; In re Danly, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959).

As for claims 18 and 19, the specification contains no disclosure of either the critical nature of the claimed arrangement or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

As for claim 20, Buchanan discloses a contact layer 5 of first conduction type interposed between the substrate and the buffer layer.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art (APA) in view of Takahashi.

The APA discloses in fig. 9 a semiconductor light-receiving device comprising: a semi-insulating substrate 111; a semiconductor layer 112 of a first conduction type or N-type (as in claim 15) that is formed on the semi-insulating substrate; a buffer layer 113 of the first conduction type that is formed on the semi-insulating substrate and has a lower impurity concentration than the semiconductor layer of the first conduction type; a light absorption layer 114 that is formed on the buffer layer and generates carriers in accordance with incident light; a semiconductor layer 117 of a second conduction type that is formed on the light absorption layer; and a semiconductor intermediate layer 115/116, but lacks anticipation of a semiconductor intermediate layer interposed between the buffer layer and the light absorption layer.

Takahashi discloses in fig. 3 a semiconductor light-receiving device comprising: a substrate; a buffer layer 2 of the first conduction type that is formed on the substrate; a light absorption layer 3 that is formed on the buffer layer; a semiconductor layer 5 of a second conduction type that is formed on the light absorption layer; and a semiconductor intermediate layer 8 that is interposed between the buffer layer and the light absorption layer, and has a forbidden bandwidth within a range lying between the forbidden bandwidth of the buffer layer and the forbidden bandwidth of the light absorption layer.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the APA by incorporating a semiconductor intermediate layer since that would prevent deterioration of light receiving characteristics as taught by Takahashi.

Regarding claim 2, the APA discloses (par. 0011) the buffer having an impurity concentration within the range recited in the claim.

Regarding claim 3, the APA discloses the semiconductor intermediate layer including a plurality of semiconductor layers, with forbidden bandwidths being varied stepwise.

Regarding claim 4, the APA discloses the semiconductor intermediate layer including a plurality of semiconductor layers, with forbidden bandwidths being periodically varied.

Regarding claim 5, the APA discloses a composition-graded semiconductor intermediate layer that is interposed between the light absorption layer 114 and the semiconductor layer 117 of the second conduction type, with forbidden bandwidths being varied stepwise.

Regarding claim 6, the APA discloses the semiconductor intermediate layer has a lower refractive index than the light absorption layer.

Regarding claim 7, the APA discloses a first electrode 119 unit that is electrically connected to the semiconductor layer of the first conduction type, with a first potential being applied to the first electrode unit; and a second electrode unit 120 that is electrically connected to the semiconductor layer of the second conduction type, a second potential being applied to the second electrode unit.

Regarding claim 8, the APA discloses the light absorption layer being an InGaAs layer; and the buffer layer being a In.sub.1-xGa.sub.xAs.sub.yP.sub.1-Y. Note that at x = 0, y = 0, the buffer layer is reduced to InP.

Regarding claim 9, the APA discloses the light absorption layer and the semiconductor layer of the second conduction type form a mesa structure, with light entering the light absorption layer through a side surface of the light absorption layer that is exposed in a process of forming the mesa structure.

Regarding claims 11 and 12, the APA discloses a PIN-type photodiode or an avalanche photodiode (as in claim 12).

Regarding claim 13, the APA discloses the semiconductor layer of the second conduction type has a light receiving surface formed thereon.

11. Claims 1, 6, 7 and 9-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishihara ("Ishihara") JP 63-124475 in view Uchida.

Ishihara discloses a semiconductor light-receiving device comprising: a semi-insulating substrate 1; a semiconductor layer 2 of a first conduction type that is formed on the semi-insulating substrate; a buffer layer 3 of the first conduction type that is formed on the semi-insulating substrate and has a lower impurity concentration than the semiconductor layer of the first conduction type; a light absorption layer 4 that is formed on the buffer layer and generates carriers in accordance with incident light; a semiconductor layer 6 of a second conduction type that is formed on the light absorption layer, but lacks anticipation of a semiconductor intermediate layer.

Uchida discloses in figs. 1 and 9 a semiconductor light-receiving device comprising: a substrate; a semiconductor layer 5 of a first conduction type or N type (as in claim 15) that is formed on the substrate; a buffer layer 4 of the first conduction type that is formed on the substrate; a light absorption layer 3a that is formed on the buffer layer; a semiconductor layer 2 of a second conduction type that is formed on the light absorption layer; and a semiconductor intermediate layer 3c that is interposed between the buffer layer and the light absorption layer, and has a forbidden bandwidth within a range lying between the forbidden bandwidth of the buffer layer and the forbidden bandwidth of the light absorption layer.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify Ishihara's device by incorporating a semiconductor intermediate layer since that would prevent excited electrons from being blocked as taught by Uchida.

Regarding claim 6, Uchida discloses the semiconductor intermediate layer has a lower refractive index than the light absorption layer.

Regarding claim 7, Uchida discloses a first electrode 10 unit that is electrically connected to the semiconductor layer of the first conduction type, with a first potential being applied to the first electrode unit; and a second electrode unit 9 that is electrically connected to the semiconductor layer of the second conduction type, a second potential being applied to the second electrode unit.

Regarding claim 9, Uchida discloses the light absorption layer and the semiconductor layer of the second conduction type form a mesa structure, with light entering the light absorption layer through a side surface of the light absorption layer that is exposed in a process of forming the mesa structure.

Regarding claim 10, Uchida discloses a semiconductor optical waveguide path 7A that is formed on the semi-insulating substrate and guides light to the light absorption layer.

Regarding claims 11 and 12, Uchida discloses a PIN-type photodiode or an avalanche photodiode (as in claim 12).

Regarding claim 13, Uchida discloses the semiconductor layer of the second conduction type has a light-receiving surface formed thereon.

Regarding claim 14, Uchida discloses the semi-insulating substrate has a light receiving surface on the bottom surface thereof.

12. Claims 17, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ajisawa et al. ("Ajisawa") USPN 5,825,047 in view of Viela et al. ("Viela") USPN 5,800,630.

Ajisawa discloses in fig. 6 a semiconductor light-receiving device comprising: a semi-insulating substrate; a buffer layer 64 of the first conduction type that is formed on the semiconductor layer; a light absorption layer 66 that is formed on the buffer layer and generates carriers in accordance with incident light; a semiconductor layer of a second conduction type 67 that is formed on the light absorption layer; a semiconductor intermediate layer 65 of the first conduction type that is interposed between the buffer layer and the light absorption layer, but lacks anticipation of a semiconductor layer of a first conduction type that is formed on the semi-insulating substrate or a semiconductor intermediate layer having a higher impurity concentration than the buffer layer.

Viela discloses in fig. 4 a semiconductor light-receiving device comprising: a semiconductor layer of a first conduction type (bottom layer) and a high-concentration semiconductor intermediate tunneling layer (third layer from bottom) having a higher impurity concentration than a buffer layer (second layer from bottom).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Viela's teachings with Ajisawa's device since that would produce a desirable characteristics of a tunnel junction as taught by Viela.

Regarding claim 21, Ajisawa discloses a light absorption layer 66 and the semiconductor layer of the second conduction type 67 form a mesa structure, with light entering the light absorption layer through a side surface of the light absorption layer that is exposed in a process of forming the mesa structure.

Regarding claim 22, Ajisawa discloses a semiconductor waveguide path formed on a semi-insulating substrate.

13. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe ("Watanabe") JP 6-90016 in view of Viela.

Watanabe discloses in fig. 5 a semiconductor light-receiving device comprising: a semiconductor substrate 21 of a first conduction type; a buffer layer 24 of the first conduction type that is formed on the semiconductor substrate and having a lower impurity concentration than the semiconductor substrate; a light absorption layer 26 that is formed on the buffer layer and generates carriers in accordance with incident light; a semiconductor layer 27 of a second conduction type that is formed on the light absorption layer; and a high-concentration semiconductor intermediate layer 25 of the first conduction type that is interposed between the buffer layer and the light absorption layer but lacks anticipation of the intermediate layer having a higher impurity concentration than the buffer layer.

Viela discloses in fig. 4 a semiconductor light-receiving device comprising: a high-concentration semiconductor intermediate tunneling layer (third layer from bottom) having a higher impurity concentration than a buffer layer (second layer from bottom).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Viela's teachings with Watanabe's device since that would produce a desirable characteristics of a tunnel junction as taught by Viela.

As to the semiconductor intermediate tunneling layer allowing electrons to pass therethrough to the buffer layer due to tunnel effect, it is a desired result rather than a structural limitation. See In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir.

1997); See also In re Swinehart, 439 F.2d210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971; In re Danly, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANS
November 10, 2005